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EXAMINER	
CHU, GABRIEL L	
ART UNIT	**PAPER NUMBER**
2114	

DATE MAILED: 08/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/084,533	DELANO, ERIC	
	Examiner	Art Unit	
	Gabriel L. Chu	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 3, 4, 9, and 20 are objected to because of the following informalities:

Referring to claims 3 and 4, "register and" is understood to refer to "register".

Referring to claim 9, "the step of re-executing" is understood to refer to "a step...", correcting for antecedence.

Referring to claim 20, "further comprising a program counter" appears to overlook the program counter already claimed in claim 12, "relative to a program counter". For the purpose of examination, this limitation is removed from claim 20.

Further referring to claim 20, "connection the" is understood to refer to "connection to the".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 2 and 8 are rejected under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which applicant(s) regard as their invention. Evidence that claim 2 fail(s) to correspond in scope with that which applicant(s) regard as the invention can be found in the reply filed 27 February 2002. In that paper, applicant has stated, from paragraph 16, amongst others, "One write port

19 may be used to write the temporary data from buffer 20 to register file 12 when data errors are detected and to re-execute a program.", and this statement indicates that the invention is different from what is defined in the claim(s) because it is not understood how, from claim 1, one can restore "in the event of data errors" and also, from claim 2 with emphasis, restore "over a period *before* checking for data errors". This is seen as contradictory as both Applicant's specification and the claim from which claim 2 depends calls for restoration following detection. Further, nowhere in the specification is restoring over a prior period before checking for data errors mentioned.

Evidence that claim 8 fail(s) to correspond in scope with that which applicant(s) regard as the invention can be found in the reply filed 27 February 2002. In that paper, applicant has stated, from the abstract, amongst others, "if there are errors, the register file is rewritten with contents from the buffer and the program counter is reset to the prior checkpoint, whereinafter processing re-executes program instructions from the last checkpoint.", and this statement indicates that the invention is different from what is defined in the claim(s) because backing up a program counter *after* fault is detected is seen to contradict resetting a program counter to the prior checkpoint. For the purpose of examination, claim 8 is understood to refer to "*restoring* a program counter..."

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 3-18, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5692121 to Bozso et al. Referring to claim 1, Bozso et al. disclose storing a backup of data for a register of a register file and within a buffer; periodically checking for data errors within the processor; and restoring the data from the buffer to the register file in the event of data errors (From line 49 of column 2, "If the outputs and their ECCs are identical, then the R-Unit checkpoints one of the copies in an architected-state array. If the outputs or the generated ECCs differ, then an error is indicated, the checkpointing operation is blocked, and recovery is effected by using the checkpointed state from the architected-state array. In the recovery action, the processors are both returned to the state that is consistent with the last successfully completed instruction.").

Referring to claim 3, Bozso et al. disclose loading new data to the register and after the step of storing (From line 60 of column 8, "Note that Cycle 3 (during which a transfer takes place from a Current State array to the Checkpoint array), corresponding to the completion of an instruction, can be concurrent with a Cycle 2 of the subsequent instruction. In other words, newly arriving state can be written into the Current State array on the same cycle as the successfully completed state change is transferred form the Current State array to the Checkpointed State array.").

Referring to claim 4, Bozso et al. disclose loading new data to the register and concurrently with the step of storing (From line 60 of column 8, "Note that

Cycle 3 (during which a transfer takes place from a Current State array to the Checkpoint array), corresponding to the completion of an instruction, can be concurrent with a Cycle 2 of the subsequent instruction. In other words, newly arriving state can be written into the Current State array on the same cycle as the successfully completed state change is transferred form the Current State array to the Checkpointed State array.").

Referring to claim 5, Bozso et al. disclose the step of storing the data within the buffer comprising storing the data within a second register file (From line 10 of column 9, "For example, the 0/1 Current State register from the Processor A side of the drawing can only go to the GR 0/1, the MGR 0/1, the HCR 0/1, or the G2CR 0/1 registers of the Checkpointed State array.").

Referring to claim 6, Bozso et al. disclose the step of flushing the buffer after checking for, and detecting no, data errors (From line 49 of column 2, "If the outputs and their ECCs are identical, then the R-Unit checkpoints one of the copies in an architected-state array." Wherein flushing is to clear a portion of memory; e.g., flushing a disk file buffer to save its contents on disk and then clear the buffer for filling again.").

Referring to claim 7, Bozso et al. disclose the step of freezing execution of instructions within pipelines of the processor after detecting data errors (From the abstract, "if an error is detected, a recovery sequence can be initiated after the check-stop operation, whereby the system is restored to the last error-free checkpointing operation.").

Referring to claims 8 and 9, Bozso et al. disclose the step of restoring a

program counter of the processor after detecting errors and a step of re-executing a program through the processor at a time associated with the backed up program counter (From line 47 of column 8, "If there is a miscompare prior to checkpointing, then the checkpointing operation is inhibited, and the processor state is recoverable to the point that is consistent with the last successful checkpoint operation. Recovery is performed by small state-machines in the I-Unit and E-Unit. The I-Unit state-machine reads all 128 registers in sequence. As each register is read, the R-Unit corrects any latent soft errors. The E-Unit state-machine updates all shadow copies of these registers (i.e., the actual working registers) from the checkpointed state, and it rewrites the checkpointed state back into the R-Unit. This completely "scrubs" the processor state, and recovers the processor to the point of the last successfully completed operation." Wherein the processor starts processing the instruction stream again from the checkpoint, arriving at a prior point in the current state of processing.).

Referring to claim 10, Bozso et al. disclose the step of periodically checking for data errors comprising periodically checking for the data errors at sequential time periods defined by a number of processor clock cycles (From line 32 of column 2, "The R-Unit compares the results (output operands) of the two processors on a cycle-by-cycle basis, and does a formal checkpointing or storing of those remits on a per-instruction basis.").

Referring to claim 11, Bozso et al. disclose the steps of utilizing an error correction code in connection with data storage to the buffer (From line 44 of column 2, "In operation, as the instructions produce outputs (storage or register-

sink operands) in the two mirror-image processors, the R-Unit generates ECCs for the pair of outputs, and compares them to determine whether the processors have successfully generated identical outputs.").

Referring to claim 12, Bozso et al. disclose an execution unit having a plurality of pipelines for processing program instructions relative to a program counter (From line 57 of column 2, "To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described, the invention provides for a recovery unit for a mirrored processor, comprising means for separately storing identical data received from each of two processors. The data includes data information and address information. The data received from each processor is partitioned into a plurality of data subsets. Error correction codes (ECCs) are partitioned for each data subset of the plurality of data subsets. An interlaced is generated entity in each processor containing the data, address, and ECC information. Corresponding data subsets of the interlaced entity of each processor are compared with their respective ECCs for errors. The data subsets are checkpointed if no errors are detected. If errors are detected, a recovery sequence is initiated."); a register file, wherein one or more stages of the pipelines loads data to a register of the register file (From line 10 of column 9, "For example, the 0/1 Current State register from the Processor A side of the drawing can only go to the GR 0/1, the MGR 0/1, the HCR 0/1, or the G2CR 0/1 registers of the Checkpointed State array."); and a buffer for storing a backup of data within the register and for restoring data to the register file in the event of data errors within the processor (From line 10 of column 9, "For

example, the 0/1 Current State register from the Processor A side of the drawing can only go to the GR 0/1, the MGR 0/1, the HCR 0/1, or the G2CR 0/1 registers of the Checkpointed State array.").

Referring to claim 13, Bozso et al. disclose the buffer comprising a second register file (From line 10 of column 9, "For example, the 0/1 Current State register from the Processor A side of the drawing can only go to the GR 0/1, the MGR 0/1, the HCR 0/1, or the G2CR 0/1 registers of the Checkpointed State array.").

Referring to claim 14, Bozso et al. disclose the register file comprising an extra read port for reading the data from the register (From line 63 of column 8, "In other words, newly arriving state can be written into the Current State array on the same cycle as the successfully completed state change is transferred form the Current State array to the Checkpointed State array. In short, any location in the Current State array can be read-from and written-to in the same cycle, and the array is constructed to allow this without corrupting the output data with the input data.").

Referring to claim 15, Bozso et al. disclose the register file comprising a write port for writing the data from the buffer to the register (From line 63 of column 8, "In other words, newly arriving state can be written into the Current State array on the same cycle as the successfully completed state change is transferred form the Current State array to the Checkpointed State array. In short, any location in the Current State array can be read-from and written-to in the same cycle, and the array is constructed to allow this without corrupting the

output data with the input data.").

Referring to claim 16, Bozso et al. disclose one or more error detectors for detecting the data errors (From line 57 of column 2, "To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described, the invention provides for a recovery unit for a mirrored processor, comprising means for separately storing identical data received from each of two processors. The data includes data information and address information. The data received from each processor is partitioned into a plurality of data subsets. Error correction codes (ECCs) are partitioned for each data subset of the plurality of data subsets. An interlaced is generated entity in each processor containing the data, address, and ECC information. Corresponding data subsets of the interlaced entity of each processor are compared with their respective ECCs for errors. The data subsets are checkpointed if no errors are detected. If errors are detected, a recovery sequence is initiated.").

Referring to claim 17, Bozso et al. disclose the error detectors comprising redundant logic devices (From line 57 of column 2, "To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described, the invention provides for a recovery unit for a mirrored processor, comprising means for separately storing identical data received from each of two processors. The data includes data information and address information. The data received from each processor is partitioned into a plurality of data subsets. Error correction codes (ECCs) are partitioned for each data subset of the plurality of data subsets. An interlaced is generated entity in each

processor containing the data, address, and ECC information. Corresponding data subsets of the interlaced entity of each processor are compared with their respective ECCs for errors. The data subsets are checkpointed if no errors are detected. If errors are detected, a recovery sequence is initiated.").

Referring to claim 18, Bozso et al. disclose error correction code for data recovery of data stored within the buffer (From line 57 of column 2, "To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described, the invention provides for a recovery unit for a mirrored processor, comprising means for separately storing identical data received from each of two processors. The data includes data information and address information. The data received from each processor is partitioned into a plurality of data subsets. Error correction codes (ECCs) are partitioned for each data subset of the plurality of data subsets. An interlaced is generated entity in each processor containing the data, address, and ECC information. Corresponding data subsets of the interlaced entity of each processor are compared with their respective ECCs for errors. The data subsets are checkpointed if no errors are detected. If errors are detected, a recovery sequence is initiated.").

Referring to claim 20, Bozso et al. disclose the program counter being reset in connection the buffer restoring data to the register file (From line 47 of column 8, "If there is a miscompare prior to checkpointing, then the checkpointing operation is inhibited, and the processor state is recoverable to the point that is consistent with the last successful checkpoint operation. Recovery is performed

by small state-machines in the I-Unit and E-Unit. The I-Unit state-machine reads all 128 registers in sequence. As each register is read, the R-Unit corrects any latent soft errors. The E-Unit state-machine updates all shadow copies of these registers (i.e., the actual working registers) from the checkpointed state, and it rewrites the checkpointed state back into the R-Unit. This completely "scrubs" the processor state, and recovers the processor to the point of the last successfully completed operation." Wherein the processor starts processing the instruction stream again from the checkpoint, arriving at a prior point in the current state of processing.).

Claim Rejections - 35 USC § 103

6. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 5692121 to Bozso et al. as applied to claim 12 above, and further in view of US 5568380 to Brodnax et al. Referring to claim 19, Bozso et al. disclose buffering the current state data so that faults may be tolerated so that operations may continue (From line 49 of column 2, "If the outputs and their ECCs are identical, then the R-Unit checkpoints one of the copies in an architected-state array. If the outputs or the generated ECCs differ, then an error is indicated, the checkpointing operation is blocked, and recovery is effected by using the checkpointed state from the architected-state array. In the recovery action, the processors are both returned to the state that is consistent with the last successfully completed instruction."). Although Bozso et al. do not explicitly disclose the buffer reading data within the register prior to an execution stage for an instruction identifying a write to the register, reading the register that needs to

be backed up prior to it being written into is known in the art. An example of this is shown by Brodnax et al., from line 16 of column 3, "When a memory write is executed, the general purpose register (GPR) values are saved in the FXP's shadow register files." A person of ordinary skill in the art at thet ime of the invention would have been motivated to save the contents that need to be backed up prior to them being written over because, from line 18 of column 3, "With saved data, the processor can be rolled back to its last known good state if an error is detected between memory writes."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 3736566 to Anderson et al.

US 5119483 to Madden et al.

US 5296017 to Hayden et al.

US 6629271 to Lee et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gabriel L. Chu whose telephone number is (703) 308-7298. The examiner can normally be reached on weekdays between 8:30 AM and 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel, Jr. can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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